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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,203	10/29/2003	Jeffrey F. Hanson	03-1433	7329
24319	7590	07/27/2005	EXAMINER	
LSI LOGIC CORPORATION			LIN, SUN J	
1621 BARBER LANE			ART UNIT	PAPER NUMBER
MS: D-106			2825	
MILPITAS, CA 95035				

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/696,203	HANSON ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 29 October 2003.
- 2a) This action is FINAL.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-20 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 10/29/2003 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    - a) All    b) Some \* c) None of:
      1. Certified copies of the priority documents have been received.
      2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
      3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                    | Paper No(s)/Mail Date: _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date: _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

1. This office action is in response to application 10/696,203 filed on 10/29/2003. Claims 1 –20 remain pending in the application.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3 – 9, 11 – 16 and 18 – 20 are rejected under 35 U.S.C. 102(b) as being unpatentable over U.S. Patent No. 6,185,707 B1 to Smith et al.

4. As to Claim 1, Smith et al. teach the following subject matter:

- Identifying X, Y- coordinate data (i.e., physical locations) of suspect defective netlist (i.e., yield enhancement data) are stored in a database to provide yield enhancement engineers a starting point performing failure analysis of integrated circuits on a substrate – [abstract; col. 3, line 37 - 62];
- Comparing a database of (suspected) defects on the substrate (wafer) to a database of design information (i.e., design database) for the integrated circuits – [abstract; col. 3, line 1, line 12];
- Associating the suspected defects on the substrate with physical traces (i.e., classes of design information – layout patterns) on the chip layout (on the substrate) to identify and produce an accurate X, Y- coordinate data of suspect defective netlist (yield enhancement data) – [col. 3, line 37 – 62].

For reference purposes, the explanations given above in response to Claim 1 are called [Response A] hereinafter.

5. As to Claim 9, in addition to reasons included in [Response A] given above, Smith et al. disclose the following subject matter:

- (Physical layout) pattern files (i.e., design files)... design information...design database – [col. 3, line 1 – 35]; Notice that design information regarding layout patterns is used as a template (i.e., guide lines) for fabricating the integrated circuits on the substrate;
- Physical locations of suspected netlist nodes (i.e., defects) are stored in a database – [col. 3, line 48 – 53]. Notice the defeats are detected in in-line inspection data, which are collected during processing of the integrated circuit.

For reference purposes, the explanations given above in response to Claim 9 are called **[Response B]** hereinafter.

6. As to Claim 16, reasons are included in **[Response A]** and **[Response B]** given above.
7. As to Claims 3 and 11, defeats on the substrate associated with the physical traces are optically observable defects.
8. As to Claims 4, 5, 12, 13, 19 and 20, the design information (physical traces) includes physical structures (i.e., layout patterns) formed in the integrated circuits. Therefore, the classes of design information comprise classes of physical structures.
9. As to Claims 6 and 14, Smith et al. disclose the following subject matter:
  - Yield enhancement...semiconductor manufacturing plants...in-line defect inspection tools – [col. 2, line 19 – 30]; notice that the in-line inspection tools are designed for use in inspection of defects on the substrate, where the inspissations are conducted at multiple times during fabrications of integrated circuits.
10. As to Claim 7, Smith et al. teach the following subject matter:
  - (Physical layout) pattern files (i.e., design files)... design information...design database – [col. 3, line 1 – 35].

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11. As to Claims 8, 15 and 18, Smith et al. teach the subject matter regarding cross mapping (i.e., revising) the circuit design information based on physical locations (i.e., yield enhancement data) defects on the substrate – [col. 3, line 38 – 62].

***Claim Rejections - 35 USC § 103***

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

- (1). Determining the scope and contents of the prior art.
- (2). Ascertaining the differences between the prior art and the claims at issue.
- (3). Resolving the level of ordinary skill in the pertinent art.
- (4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. Claims 2, 10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,185,707 B1 to Smith et al. in view of U.S. Patent No. 6,542,830 B1 to Mizuno et al.

14. As to Claim 2, Smith et al. teach a method of storing defects on a substrate of integrated circuits in a database, they do not teach that database of defects comprises a defect wafer map. But Mizuno et al. show and teach the subject matter in Fig. 5, Fig. 6 and Fig. 7. Mizuno et al. teach that a defect map is formed by plotting (defect) results retrieved from inspection data based on a wafer map to make a defect state on the wafer visually clear.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of Mizuno et al. in forming a defect wafer map by plotting (defect) results retrieved from inspection data

stored in a defect database in order to make a defect state on the wafer to be visually clear to be reviewed by a yield enhancement engineer.

For reference purposes, the explanations given above in response to Claim 2 are called [Response C] hereinafter.

15. As to Claims 10 and 17, reasons are included in [Response C] given above.

### ***Conclusion***

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin  
Patent Examiner  
Art Unit 2825  
July 23, 2005

